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EXAMINER	
STOREY, WILLIAM C	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,910	GRAF ET AL.	
	Examiner	Art Unit	
	WILLIAM C. STOREY	4115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/1/07 & 5/9/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 6, 15, 24, 34, 42, and any other similarly-worded claims are objected to because of the following informalities: "Error bit comprises....horizontal parity code, and vertical parity code" is taken to read "error bit comprises....horizontal parity code, or vertical parity code." Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 10, & 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Skene et al. (US Patent 6616260), hereinafter referred to as Skene.

Regarding claim 1, Skene discloses communication between a printhead and a controller, which reads on claimed print host, print host coupled to a print head, communicating a first data stream between the printer host and the print head; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits in data that are to be communicated in order to detect possible errors, which reads on claimed inserting a reference data stream into the first data stream; as disclosed at column 7, lines 55-58. Skene discloses checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed validating the first data stream based on the reference data stream; as disclosed at column 8, lines 41-45, for example.

Regarding claim 4, Skene discloses everything as applied above for claim 1. Skene discloses memory integrated with the inkjet printhead assembly, as disclosed in column 3, lines 58-59. Bits, which read on claimed data, are located in the memory, as disclosed in column 3, lines 48-49. A controller causes the reading of data from the memory as disclosed above, causing the data to be sent and thus, received. The parity bit, which reads on claimed reference data stream, is inserted into the list of bits being communicated in the claimed first data stream, as disclosed above. This reads on claimed transmitting a print head data stream comprising the first data stream and the reference data stream from the print head; and receiving the print head data stream at the printer host.

Regarding claim 10, Skene discloses everything as applied above in claim 1. Skene discloses memory integrated with the inkjet printhead assembly, as disclosed in column 3, lines 58-59. Bits excluding a parity bit, which read on claimed first data stream, are located in the memory, as disclosed in column 3, lines 48-49. A controller causes the reading of data from the memory as disclosed above. This reads on claimed retrieving the first data stream stored in a print head memory.

Regarding claim 20, Skene discloses communication between an inkjet printhead and a controller, which reads on claimed host, print head communication link coupling the print head and the host, and configured to communicate a first data stream between the print head and the host; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits, which reads on claimed insert a reference data stream; in data that are to be communicated, which reads on claimed first data stream; in order to

detect possible errors, which reads on claimed error detection; as disclosed at column 7, lines 55-58. Skene discloses memory integrated with the inkjet printhead assembly, which reads on claimed data stream register coupled to the print head; as disclosed in column 3, lines 58-59. Bits, which read on claimed data stream, are located in the memory and a parity bit is set based on a pattern in order to check for errors, as disclosed in column 3, lines 48-49 and column 7, lines 55-67 & column 8, lines 1-8. Skene discloses the controller checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed data validating controller coupled to the host, and configured to validate the first data stream based on the reference stream; as disclosed at column 8, lines 35-36 & 41-45, for example.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 3, 5, 6, 11-16, 19, 21-24, 28-30, & 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth et al. (US 3975712), hereinafter referred to as Hepworth.

Regarding claim 2, Skene discloses everything as applied above for claim 1. Skene discloses individual lines for individual bits, as disclosed in column 3, lines 66-67 and column 4 lines 1-10. However, Skene fails to disclose wherein the first data stream

comprises a serial data stream. However, the examiner maintains that it was well known in the art to provide wherein the first data stream comprises a serial data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses data being converted from a parallel transmittal form into a serial transmittal form, which reads on claimed wherein the first data stream comprises a serial data stream; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the first data stream comprises a serial data stream, as taught by Hepworth, for the purpose of reducing package size.

Regarding claim 3, Skene discloses everything as applied above for claim 1. However, Skene fails to disclose wherein the act of communicating the first data stream further comprises the act of synchronously communicating the first data stream. However, the examiner maintains that it was well known in the art to provide wherein the act of communicating the first data stream further comprises the act of synchronously communicating the first data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses data being transmitted through shift register based on a clock signal, which reads on claimed wherein the act of communicating the first data stream further comprises the act of

synchronously communicating the first data stream; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the act of communicating the first data stream further comprises the act of synchronously communicating the first data stream, as taught by Hepworth, for the purpose of reducing latency.

Regarding claim 5, Skene discloses everything as applied above for claim 1. The parity bit, which reads on claimed reference data stream, is inserted into the list of bits being communicated in the claimed first data stream, as disclosed above. However, Skene fails to disclose wherein the act of inserting the reference data stream further comprises the act of adding to the first data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit. However, the examiner maintains that it was well known in the art to provide wherein the act of inserting the reference data stream further comprises the act of adding to the first data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses that when the data is ready to be transmitted, inserting a start bit and a trailing stop bit or bits and that a parity may be included, which reads on claimed wherein the act of inserting the reference data stream further comprises the act of adding to the first data stream at least one of a

plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as disclosed in column 7, lines 23-30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the act of inserting the reference data stream further comprises the act of adding to the first data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as taught by Hepworth, for the purpose of enunciating the end of a transmission.

Regarding claim 6, Skene and Hepworth disclosed everything as applied above for claim 5. Skene and Hepworth both disclosed the use of a parity code above, which reads on claimed wherein the error detection bit comprises at least one of a parity check code, residue code, "m" of "n" code, duplication code, cyclic code, arithmetic code, Berger code, Hamming code, horizontal parity code, and vertical parity code.

Regarding claim 11, Skene discloses communication between a inkjet printhead and a controller, which reads on claimed inkjet printing apparatus having a printer host coupled to a print head; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits in data that are to be communicated in order to detect possible errors, as disclosed at column 7, lines 55-58. Skene discloses checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed searching for a validating data stream from the received data stream; and validating the received data stream when validating data stream comprises a valid data stream; as disclosed at column 8, lines 41-45, for example.

However, Skene fails to disclose synchronously receiving a data stream. However, the examiner maintains that it was well known in the art to provide synchronously receiving a data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses data being transmitted through shift register with start and stop bits, as disclosed at column 7, lines 23-30. Hepworth discloses the data being received and that the start bit synchronizes the timing of the data being received, as disclosed at column 7, lines 46-50. This read s on claimed synchronously receiving a data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing synchronously receiving a data stream, as taught by Hepworth, for the purpose of increased accuracy.

Regarding claim 12, Skene and Hepworth disclose everything as applied above for claim 11. However, Skene fails to disclose wherein the data stream comprises a serial data stream. However, the examiner maintains that it was well known in the art to provide wherein the data stream comprises a serial data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses the data above being serialized for transfer, as disclosed at column 7, lines 23-30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the data

stream comprises a serial data stream, as taught by Hepworth, for the purpose of reducing package size.

Regarding claim 13, Skene and Hepworth disclose everything as applied above for claim 11. As disclosed above, receiving a data stream read on claimed retrieving a data stream. Skene and Hepworth disclose above inserting bits such as parity or start and stop bits, which reads on claimed reference data stream; into the original data stream, which reads on claimed first data stream.

Regarding claim 14, Skene and Hepworth disclose everything as applied above for claim 13. Hepworth disclose above that when the data is ready to be transmitted, inserting a start bit and a trailing stop bit or bits and that a parity may be included, which reads on claimed wherein the act of inserting the reference data stream further comprises the act of adding to the first data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as disclosed in column 7, lines 23-30.

Regarding claim 15, Skene and Hepworth disclose everything as applied above for claim 14. Parity disclosed above reads on claimed parity check code, which reads on claim 15.

Regarding claim 16, Skene and Hepworth disclose everything as applied above for claim 13. Hepworth disclosed above inserting stop, start, and parity bits. Skene disclosed using a parity bit, which reads on claimed reference data stream; to detect errors, as disclosed in column 8, lines 41-45. Skene discloses odd and even patterns, which read on disclosed reference pattern; that the bit must be matched to in order to

determined validity, which reads on claimed wherein the reference data stream has a reference pattern and wherein the act of validating the received data stream comprises matching the reference pattern with the valid data pattern; as disclosed at column 8, lines 9-17 and 41-45.

Regarding claim 19, Skene discloses everything as applied above in claim 11. Skene discloses memory integrated with the inkjet printhead assembly, as disclosed in column 3, lines 58-59. Bits excluding a parity bit, which read on claimed first data stream, are located in the memory, as disclosed in column 3, lines 48-49. A controller causes the reading of data from the memory as disclosed above. This reads on claimed retrieving the first data stream stored in a print head memory.

Regarding claim 21, Skene discloses everything as applied above for claim 20. Skene discloses individual lines for individual bits, as disclosed in column 3, lines 66—7 and column 4 lines 1-10. However, Skene fails to disclose wherein the first data stream comprises a serial data stream. However, the examiner maintains that it was well known in the art to provide wherein the first data stream comprises a serial data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses data being converted from a parallel transmittal form into a serial transmittal form, which reads on claimed wherein the first data stream comprises a serial data stream; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Skene by specifically providing wherein the first data stream comprises a serial data stream, as taught by Hepworth, for the purpose of reducing package size.

Regarding claim 22, Skene discloses everything as applied above for claim 20. However, Skene fails to disclose wherein the print head communication link communicates the first data stream synchronously. However, the examiner maintains that it was well known in the art to provide wherein the print head communication link communicates the first data stream synchronously, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses data being transmitted through shift register based on a clock signal, which reads on claimed wherein the print head communication link communicates the first data stream synchronously; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the print head communication link communicates the first data stream synchronously, as taught by Hepworth, for the purpose of reducing latency.

Regarding claim 23, Skene discloses everything as applied above for claim 20. The parity bit is inserted into the list of bits being communicated in the claimed first data stream in the register, as disclosed above. However, Skene fails to disclose wherein the data stream register adds at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit to the first data stream.

However, the examiner maintains that it was well known in the art to provide wherein the data stream register adds at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit to the first data stream, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses that when the data is ready to be transmitted, the information in the data register is sent to the transmit shift register and inserted are a start bit and a trailing stop bit or bits and a parity may be included, which reads on claimed wherein the data stream register adds at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit to the first data stream, as disclosed in column 7, lines 23-30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the data stream register adds at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit to the first data stream, as taught by Hepworth, for the purpose of enunciating the end of a transmission.

Regarding claim 24, Skene and Hepworth disclosed everything as applied above for claim 23. Skene and Hepworth both disclosed the use of a parity code above, which reads on claimed wherein the at least one error detection bit comprises at least one of a parity check code, residue code, "m" of "n" code, duplication code, cyclic code, arithmetic code, Berger code, Hamming code, horizontal parity code, and vertical parity code.

Regarding claim 28, claim 28 is rejected base on prior reasoning disclosed above in claim 3 and claim 1. Hepworth taught synchronous transmittal. Skene discloses communication between a printhead and a controller, which reads on claimed print controller adapted to be coupled to the print head and print head configured to transmit a data stream; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits, which reads on claimed data pattern; in data that are to be communicated in order to detect possible errors, as disclosed at column 7, lines 55-58. Skene discloses checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed validating the received data stream when the validating data stream comprises a valid data data pattern; as disclosed at column 8, lines 41-45, for example. In order to validate the transmitted stream, which reads on claimed transmitted and received data stream; based on the parity code, which reads on claimed validating data stream; that parity code bit must be found, which means it has have been searched for. Skene discloses the parity code being checked against different odd or even patterns or else the stream will not be valid, which reads on claimed validating data stream comprises a valid data stream; as disclosed at column 3, lines 48-49 and column 7, lines 55-67 & column 8, lines 1-8.

Regarding claim 29, claim 29 is rejected based on reasoning supplied above for claim 2.

Regarding claim 30, claim 30 is rejected based on reasoning supplied above for claim 4.

Regarding claim 32, claim 32 is rejected based on reasoning supplied above for

claim 1. Skene discloses setting parity bits in data that are to be communicated in order to detect possible errors, which reads on claimed inserting a reference data stream into the first data stream; as disclosed at column 7, lines 55-58. This is done in the memory in the printhead, as disclosed at column 7, lines 55-58.

Regarding claim 33, claim 33 is rejected based on reasoning supplied above for claim 5. It has already been disclosed above for the printhead to add bits and the printhead has the capability to have components integrated as disclosed with the memory. This reads on claimed printhead adds to the first data stream.

Regarding claim 34, claim 34 is rejected based on reasoning supplied above for claim 6.

Regarding claim 35, claim 35 is rejected based on reasoning supplied above for claim 16. Skene discloses the controller comparing the parity code with the pattern it should match to, which reads on claimed wherein the print controller compares the reference pattern with the valid data pattern; as disclosed at column 8, lines 36-37.

6. Claims 7 & 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and further in view of Ono et al. (US 6943911), hereinafter referred to as Ono.

Regarding claim 7, Skene and Hepworth disclose everything as applied above for claim 5. However, Skene and Hepworth fail to disclose wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values. However, the examiner maintains that it was well known in the art to provide wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values, as

taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses a start bit constituted by two bits consisting of an H level and an L level, which reads on claimed at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and thus wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values; as disclosed at column 5, line 67 and column 6, lines 1-2. H and L read on two different voltage values.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

Regarding claim 17, Skene and Hepworth disclose everything as applied above for claim 13. The examiner maintains that it was well known in the art to provide wherein inserting a reference data stream comprises the act of forming the reference data stream with a data stream independent of the first data stream, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data stream; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bits will always be comprised of an H

level and an L level, this reads on claimed wherein inserting a reference data stream comprises the act of forming the reference data stream with a data stream independent of the first data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing wherein inserting a reference data stream comprises the act of forming the reference data stream with a data stream independent of the first data stream, as taught by Ono, for the purpose of signaling the start of the data being transmitted for effect.

Regarding claim 18, Skene and Hepworth disclose everything as applied above for claim 11. However, Skene and Hepworth fail to disclose wherein validating the received data stream comprises the act of checking the reference data stream for a non-uniform bit pattern. However, the examiner maintains that it was well known in the art to provide wherein validating the received data stream comprises the act of checking the reference data stream for a non-uniform bit pattern, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data stream; constituted by an H and an L level before the data being transmitted for effect (which together read on claimed received data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bit is composed of two different levels, this reads on claimed forming the reference stream with a non-uniform bit pattern. Ono discloses using a start bit detecting terminal, as disclosed at column 6, lines 22-56. If the start bits which comprise the start information

is not found, then the proceeding information will not be read or interpreted, which reads on claimed validating, by the necessitation of matching that start pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing wherein validating the received data stream comprises the act of checking the reference data stream for a non-uniform bit pattern, as taught by Ono, for the purpose of allowing for more accuracy.

7. Claims 8-9, 26-27, & 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Ono.

Regarding claim 8, Skene discloses everything as applied above for claim 1. However, Skene fails to disclose forming the reference stream with a plurality of bits independent of the first data stream. However, the examiner maintains that it was well known in the art to provide forming the reference stream with a plurality of bits independent of the first data stream, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bits will always be comprised of an H level and an L level, this reads on claimed forming the reference stream with a plurality of bits independent of the first data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Skene by specifically providing forming the reference stream with a plurality of bits independent of the first data stream, as taught by Ono, for the purpose of signaling the start of the data being transmitted for effect.

Regarding claim 9, Skene discloses everything as applied above for claim 1. However, Skene fails to disclose forming the reference stream with a non-uniform bit pattern. However, the examiner maintains that it was well known in the art to provide forming the reference stream with a non-uniform bit pattern, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting a start bit, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bit is composed of two different levels, this reads on claimed forming the reference stream with a non-uniform bit pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a non-uniform bit pattern, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

Regarding claim 26, Skene discloses everything as applied above for claim 20. However, Skene fails to disclose forming the reference stream with a non-uniform bit pattern. However, the examiner maintains that it was well known in the art to provide forming the reference stream with a non-uniform bit pattern, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and

driving control method. In addition, Ono discloses inserting a start bit, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bit is composed of two different levels, this reads on claimed forming the reference stream with a non-uniform bit pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a non-uniform bit pattern, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

Regarding claim 27, Skene discloses everything as applied above for claim 20. However, Skene fails to disclose forming the reference stream with a data stream independent of the first data stream. However, the examiner maintains that it was well known in the art to provide forming the reference stream with a data stream independent of the first data stream, as taught by Ono.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data stream; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bits will always be comprised of an H level and an L level, this reads on claimed forming the reference stream with a data stream independent of the first data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Skene by specifically providing forming the reference stream with a data stream independent of the first data stream, as taught by Ono, for the purpose of signaling the start of the data being transmitted for effect.

Regarding claim 36, claim 36 is rejected based on reasoning supplied above for claim 9. The bits could be added before transmittal at the print head.

Regarding claim 37, claim 37 is rejected based on reasoning supplied above for claim 8. The bits could be added before transmittal at the print head.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Barbour et al. (US 6476928), hereinafter referred to as Barbour.

Regarding claim 25, Skene discloses everything as applied above for claim 20. The examiner maintains that it was well known in the art to provide a print head retrieving a first data stream from a print head memory, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable to one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing a print head retrieving a first data stream from a print head memory, as taught by Barbour, for the purpose of processing the data before sending it out to the main controller.

9. Claims 31, 38-39, 41-42, & 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and further in view of Barbour et al. (US 6476928), hereinafter referred to as Barbour.

Regarding claim 31, Skene and Hepworth disclose everything as applied above for claim 28. The examiner maintains that it was well known in the art to provide a print head retrieving a first data stream from a print head memory, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable to one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing a

print head retrieving a first data stream from a print head memory, as taught by Barbour, for the purpose of processing the data before sending it out to the main controller.

Regarding claim 38, claim 38 is rejected based on reasoning applied above for claims 1 & 4. It is well known for a print head to be used in a printing apparatus. The parity bit is inserted into the list of bits being communicated in the claimed first data stream in the register, as disclosed above. In order for the received data stream to be validated, the parity code must be correct, which reads on claimed upon receiving a data stream, can validate the received data stream if the received data stream comprises the transmit data stream with the inserted reference data stream. Transmit data stream and received data stream are equivalent and equal the first data stream plus the reference data stream. However, Skene fails to disclose inserting a reference data stream into the first data stream after the first data stream has been taken from a memory. However, the examiner maintains that it was well known in the art to provide inserting a reference data stream into the first data stream after the first data stream has been taken from a memory, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses that when the data is ready to be transmitted, the information in the data register, which reads on claimed memory; is sent to the transmit shift register and inserted are a start bit and a trailing stop bit or bits and a parity may be included, which reads on claimed inserting a reference data stream into the first data stream after the first data stream has been taken from a memory, as disclosed in column 7, lines 23-30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing inserting a reference data stream into the first data stream after the first data stream has been taken from a memory, as taught by Hepworth, for the purpose of enunciating the end of a transmission.

In addition, the examiner maintains that it was well known in the art to provide printhead comprising a data stream module adapted to retrieve the first data stream from the memory and to transmit the data stream to the host, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable for one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45, which reads on claimed transmit the data stream to the host.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing a print head retrieving a first data stream from a print head memory, as taught by Barbour,

for the purpose of processing the data before sending it out to the main controller.

A "data stream module" is simply a delineation for providing a specified function. Thus, by performing the functions disclosed above and recited in the claim, data stream module is read upon.

Regarding claim 39, Skene, Hepworth, and Barbour disclose everything as applied above for claim 38. Hepworth disclosed above that when the data is ready to be transmitted, the information in the data register, which reads on claimed memory; is sent to the transmit shift register, which reads on claimed data stream register; and inserted are a start bit and a trailing stop bit or bits and a parity may be included, which reads on claimed data stream module comprising a data stream register adapted to insert the reference data stream.

Regarding claim 41, inherits from claim 38 and claim 41 is rejected upon the reasoning provided in claim 5.

Regarding claim 42, inherits from claim 41 and claim 42 is rejected upon the reasoning provided in claim 6.

Regarding claim 44, inherits from claim 38 and claim 44 is rejected upon the reasoning provided in claim 12.

Regarding claim 45, inherits from claim 38 and claim 45 is rejected upon the reasoning provided in claim 11. Skene fails to disclose communicating the data stream synchronously. However, the examiner maintains that it was well known in the art to provide communicating the data stream synchronously, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous

communication interface adaptor. In addition, Hepworth discloses data being transmitted through shift register with start and stop bits, as disclosed at column 7, lines 23-30. Hepworth discloses the data being received and that the start bit synchronizes the timing of the data being received, as disclosed at column 7, lines 46-50. Thus, having the reception synchronized reads on claimed communicates the data stream synchronously.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing communicating the data stream synchronously, as taught by Hepworth, for the purpose of increased accuracy.

This taught form of communication may be implemented from the print head with the first data stream.

10. Claims 40 & 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth in view of Barbour and further in view of Ono.

Regarding claim 40, claim 40 is rejected upon the reasoning provided in claim 9. Bits read on claimed data stream.

Regarding claim 43, claim 43 is rejected upon the reasoning provided in claim 8. Bits read on claimed data stream.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Niimura et al. (US 6644770) discloses a printing apparatus, control method of the apparatus, and computer-readable memory. Akitaya et al. (US

2003/0095158) discloses a printer. Walker et al. (US 6718491) discloses a coding method and coder for coding packetized serial data with low overhead. Kawanabe et al. (US 2001/0015818) discloses a system for scheduling an event in a device. Walmsley et al. (US 2006/0082609) discloses compensation for horizontal skew between adjacent rows of nozzles on a printhead module. Silverbrook (US 2004/0246503) discloses a printing cartridge with radio frequency identification. Walmsley et al. (US 7165824) discloses dead nozzle compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM C. STOREY whose telephone number is (571)270-3576. The examiner can normally be reached on Monday - Friday (Alternate Fridays off) 7:30-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jefferey F. Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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